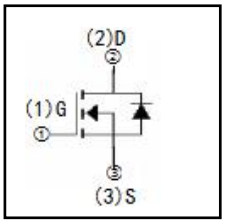
4A 800V N-channel Enhancement Mode Power MOSFET

1 Description

B4N80 , the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-251B, which accords with the RoHS standard.



V_{DSS} = 800V

I_D = 4.0A

$R_{DS(on)}$ (TYP)= 3.7Ω

2 Features

- Fast Switching
- Low ON Resistance(Rdson≤4.0Ω)
- Low Gate Charge (Typical Data:17.3 nC)
- Low Reverse transfer capacitances(Typical: 4.3pF)
- 100% Single Pulse avalanche energy Test

3 Applications

- Power switch circuit of adaptor and charger.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings (Tc=25℃,unless otherwise noted)

PARAMETER		SYMBOL	VALUE	UNIT
Drian-Source Voltage		V_{DS}	800	V
Gate-Source Voltage		V_{GS}	±30	V
Drain Current(continuous)(Note 3)		I_D	4	A
Drain Current(continuous)(T=100℃)(Note 3)		I_D	2.5	A
Drain Current(Pulsed)		I_{DM}	16	A
Single Pulse Avalanche Energy(Note 4)		E_{AS}	153	mJ
Maximum Power Dissipation	T_a=25℃	P_{tot}	1.3	W
	T_C=25℃	P_{tot}	150	W
Operating Junction Temperature Range		T_j	-55～150	℃
Storage Temperature Range		T_{stg}	-55～150	℃
High Temperature(tin solder)		T_L	300	℃

4.2 Thermal Characteristics

PARAMETER	SYMBOL	VALUE	UNIT
Thermal Resistance, Junction to Case-sink	R_{thJC}	0.8	℃/W
Thermal Resistance, Junction to Ambient	R_{thJA}	100	℃/W

4.3 Electrical Characteristics (Tc=25℃,unless otherwise noted)

PARAMETER	SYMBOL	Test Condition	VALUE			UNIT
			MIN	TYP	MAX	
Off Characteristics						
Drain-source Breakdown Voltage	BV_{DSS}	I_D=250μA,V_{GS}=0V	800	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=800V,V_{GS}=0V, T_C=25℃	--	--	25	μA
		V_{DS}=640V,V_{GS}=0V, T_C=125℃	--	--	250	μA
Gate-to-Body Leakage Current	I_{GSS}	V_{GS}=±30V,V_{DS}=0V	--	--	±100	nA
On Characteristics(Note 3)						
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.0	--	4.0	V
Drain-source on Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=2.0A	--	3.7	4.0	Ω
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{GS}=0V,V_{DS}=25V, f=1.0MHz	--	567	--	pF
Output Capacitance	C_{oss}		--	48	--	
Reverse Transfer Capacitance	C_{rss}		--	4.3	--	
Turn-on Delay Time	$T_{d(on)}$	I_D=4A, V_{DD}=400V, V_{GS}=10V, R_G=10Ω	--	11.6	--	ns
Turn-on Rise Time	t_r		--	9.5	--	
Turn-off Delay Time	$T_{d(off)}$		--	22.7	--	
Turn-off Fall	t_f		--	14	--	
Total Gate Charge	Q_g	I_D=4A,V_{DD}=640V, V_{GS}=10V	--	17.3	--	nc
Gate-to-Source Charge	Q_{gs}		--	2.6	--	
Gate-to-Drain(“Miller”)C harge	Q_{gd}		--	9.9	--	
Drain-Source Diode Characteristics						
Diode Forward Voltage(Note 3)	V_{FSD}	V_{GS}=0V,I_S=4A	--	--	1.5	V
Continuous Source Current (BodyDiode)(Note 3)	I_S		--	--	4	A
Reverse Recovery Time	t_{rr}	T_J=25℃ ,IF=4A, dIF/dt=100A/μS,VGS=0V	--	531	--	ns
Reverse Recovery Charge	Q_{rr}		--	2370	--	nc

Notes：

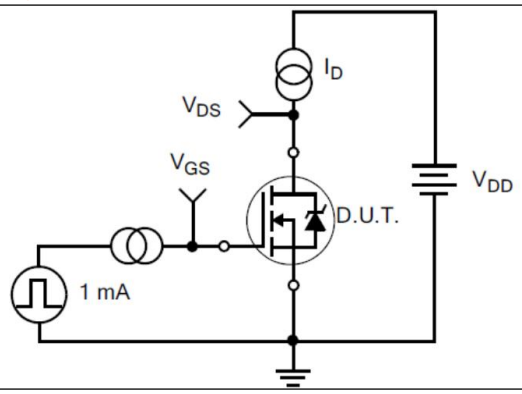
1: Repetitive rating, pulse width limited by maximum junction temperature.

2: Surface mounted on FR4 Board, t≤10sec.

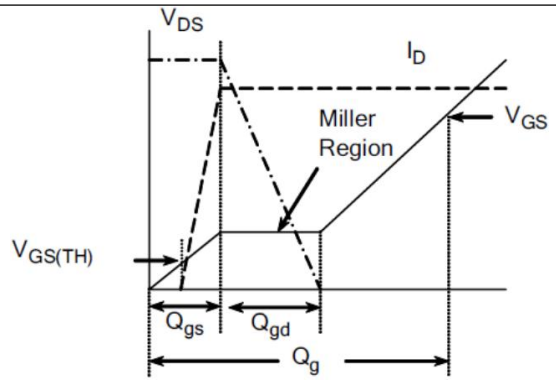
3: Pulse width ≤ 300μs, duty cycle ≤ 2%.

4: L=10 mH,I_D=5.5A,V_{DD}=50V,,Start T_J=25℃.

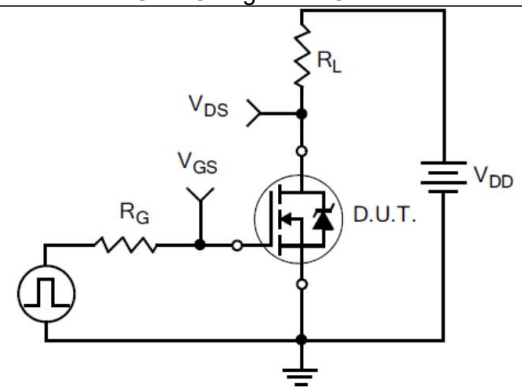
5 Typical Test Circuit and Waveform



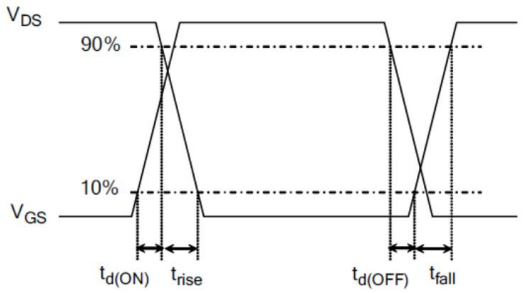
Gate Charge Test Circuit



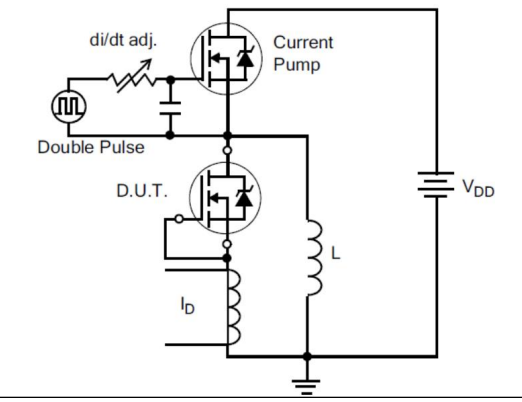
Gate Charge Waveforms



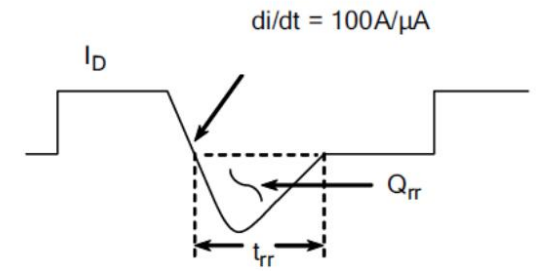
Resistive Switching Test Circuit



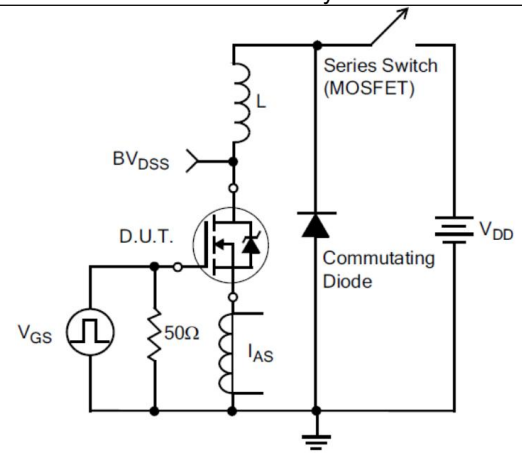
Resistive Switching Waveforms



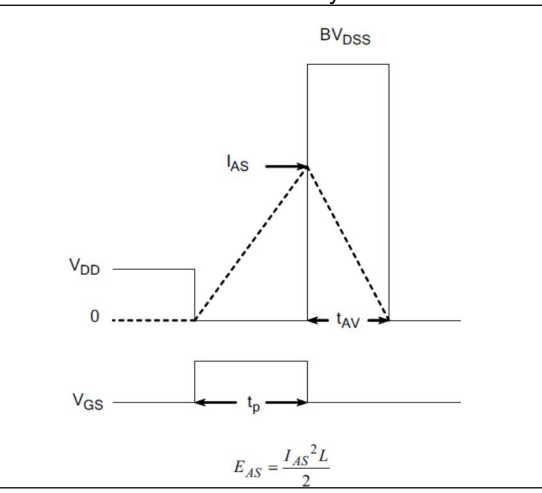
Diode Reverse Recovery Test Circuit



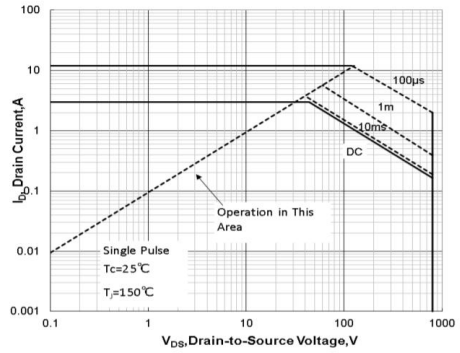
Diode Reverse Recovery Waveform



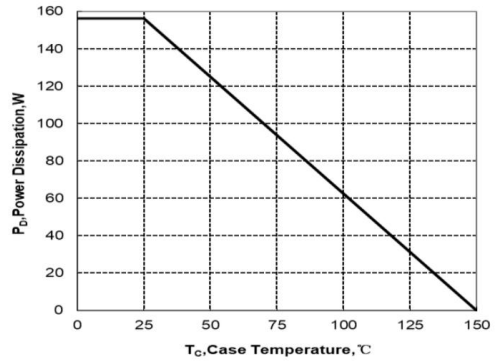
Unclamped Inductive Switching Test Circuit



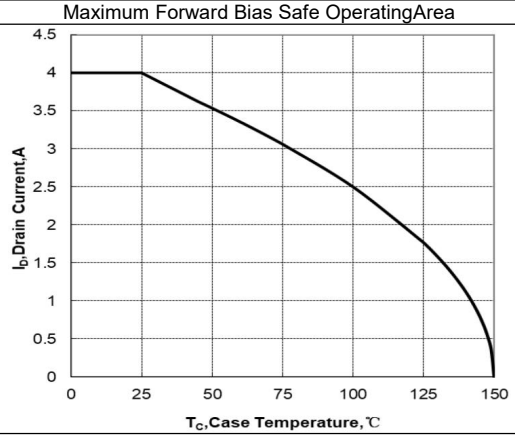
Unclamped Inductive Switching Waveform



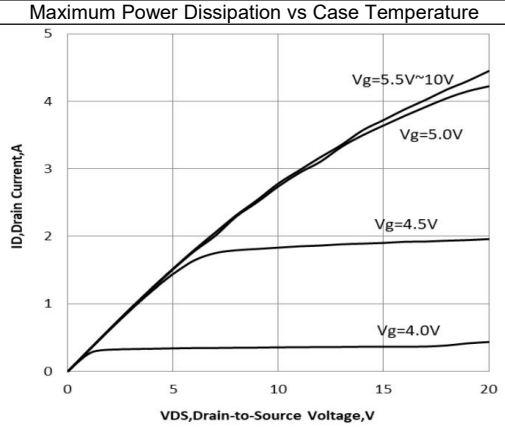
Maximum Forward Bias Safe OperatingArea



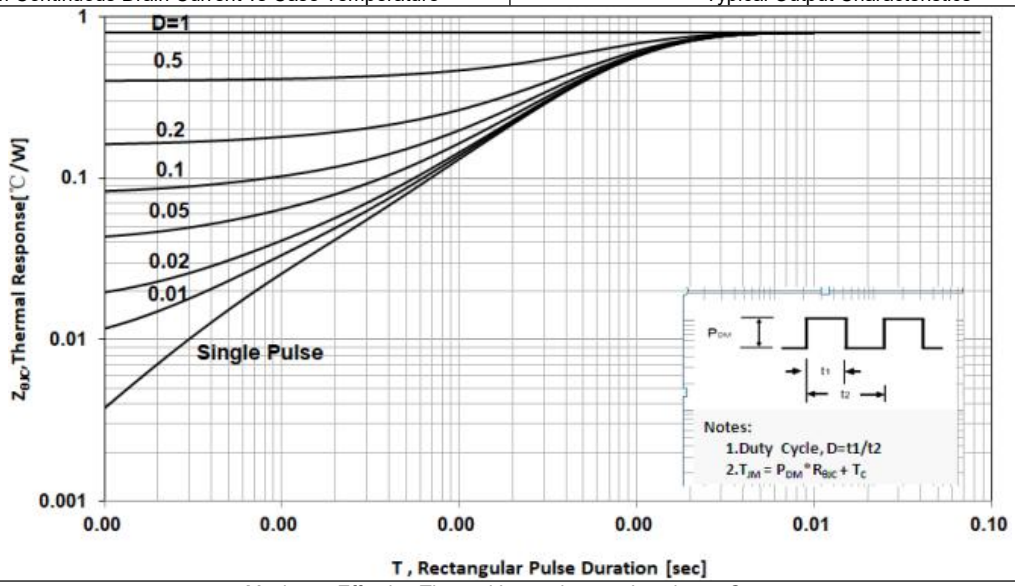
Maximum Power Dissipation vs Case Temperature



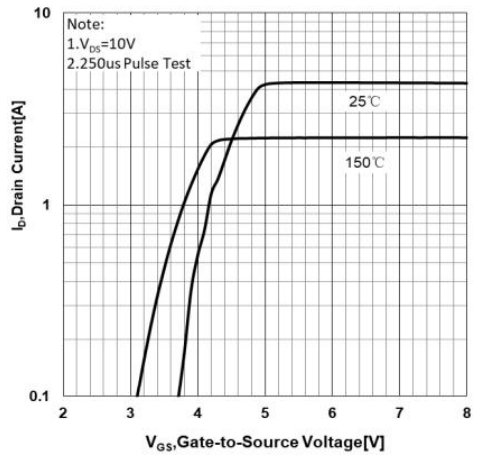
Maximum Continuous Drain Current vs Case Temperature



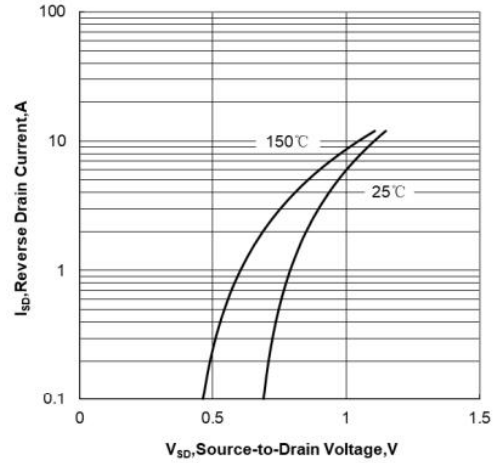
Typical Output Characteristics



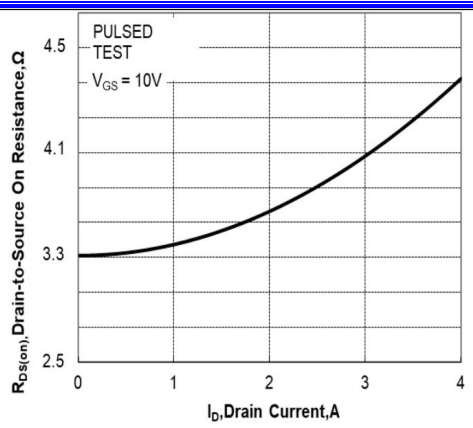
Maximum Effective Thermal Impendance , Junction to Case



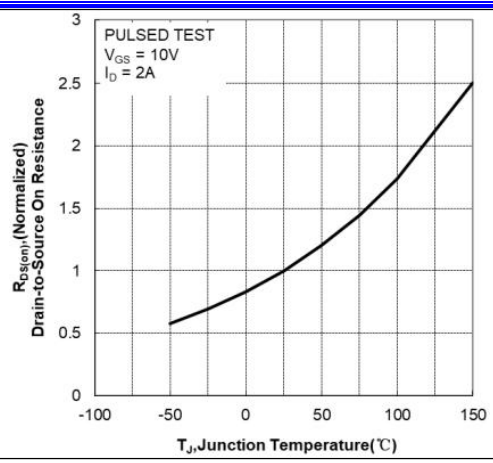
Typical Transfer Characteristics



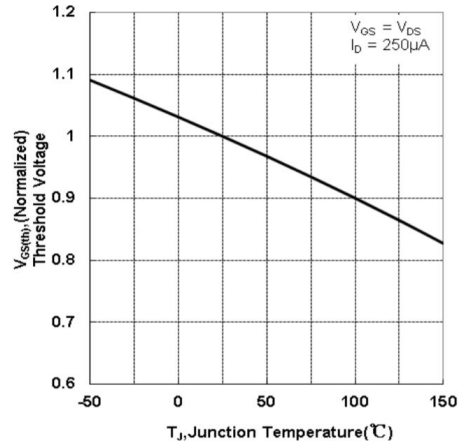
Typical Body Diode Transfer Characteristics



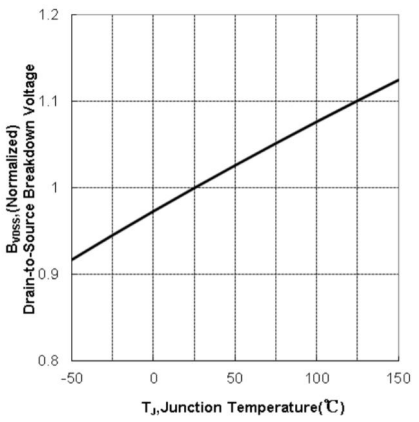
Typical Drain to Source ON Resistance vs Drain Curren



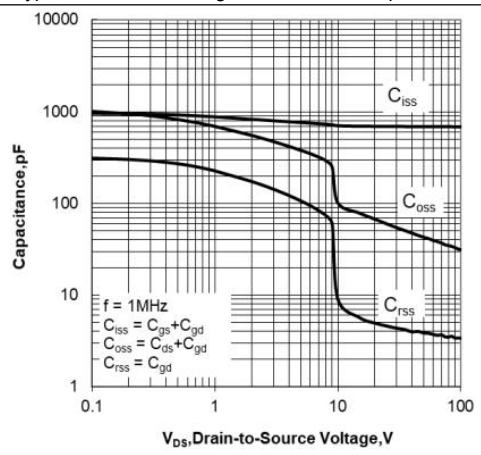
Typical Drian to Source on Resistance vs Junction Temperature



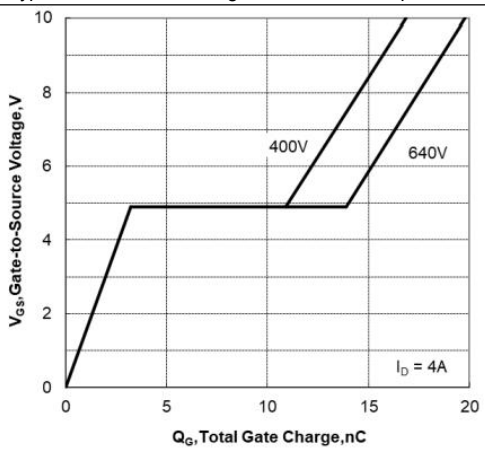
Typical Theshold Voltage vs Junction Temperature



Typical Breakdown Voltage vs Junction Temperature



Typical Capacitance vs Drain to Source Voltage

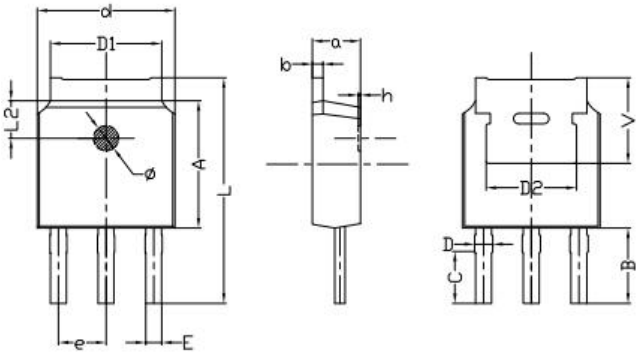


Typical Gate Charge vs Gate to Source Voltage

6 Product Specifications and Packaging Models

Product Model	Package Type	Mark Name	RoHS	Package	Quantity
B4N80	TO-251B	B4N80	Pb-free	Braid	3000/disc

7 Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	min.	max.	min.	max.
a	2.20	2.40	0.087	0.0946
b	0.46	0.58	0.018	0.023
C	2.45	2.65	0.097	0.104
D	0.80	0.90	0.032	0.035
d	6.50	6.70	0.2561	0.2640
D1	5.10	5.46	0.201	0.215
D2	4.73	4.93	0.1864	0.1942
A	6.00	6.20	0.2364	0.2443
e	2.186	2.386	0.0861	0.0940
L	10.40	11.00	0.4098	0.4334
B	3.50	3.70	0.1379	0.1458
L2	1.50	1.70	0.0591	0.0670
Φ	1.10	1.30	0.0433	0.0512
h	0.00	0.30	0.0000	0.0118
V	5.25	5.45	0.2069	0.2147
E	0.60	0.80	0.0236	0.0315

8 Attentions

- Jiangsu Donghai Semiconductor Technology Co., Ltd. reserves the right to change the specification without prior notice! The customer should obtain the latest version of the information before making the order and verify that the information is complete and up to date.
- It is the responsibility of the purchaser for any failure or failure of any semiconductor product under certain conditions. It is the responsibility of the purchaser to comply with safety standards and to take safety measures in the system design and machine manufacturing of WXDH products in order to avoid potential risk of failure. Injury or property damage.
- Product promotion is endless, our company will be dedicated to provide customers with better products.

9 Appendix

Revision history:

Date	REV.	Description	Page
2020.11.25	1.0	Original	