

## 5A 650V N-channel Enhancement Mode Power MOSFET

### 1 Description

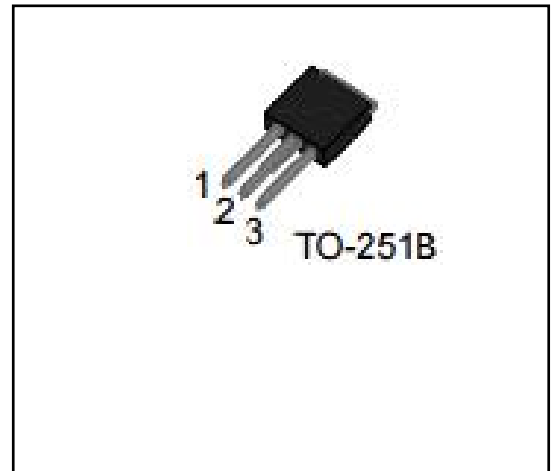
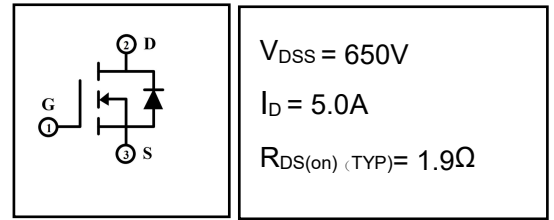
These N-channel enhanced vdmofets, is obtained by the self-aligned planar technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. Which accords with the RoHS standard.

### 2 Features

- Fast switching
- ESD improved capability
- Low on resistance( $R_{DS(on)} \leq 2.4\Omega$ )
- Low gate charge(Typ: 17.3nC)
- Low reverse transfer capacitances(Typ: 6.88pF)
- 100% single pulse avalanche energy test
- 100%  $\Delta V_{DS}$  test

### 3 Applications

- Used in various power switching circuit for system miniaturization and higher efficiency.
- Power switch circuit of electron ballast and adaptor.



## 4 Electrical Characteristics

### 4.1 Absolute Maximum Ratings (Tc=25°C, unless otherwise noted)

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	$V_{DS}$	650	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	V
Drain Current(continuous) <sup>(Note 3)</sup>	$I_D$	5	A
Drain Current(continuous)(T=100°C) <sup>(Note 3)</sup>	$I_D$	3.1	A
Drain Current(Pulsed)	$I_{DM}$	18	A
Single Pulse Avalanche Energy <sup>(Note 4)</sup>	$E_{AS}$	240	mJ
Derating Factor above	$T_a = 25^\circ C$	0.6	W
Power Dissipation	$T_C = 25^\circ C$		
Operating Junction Temperature Range	$T_j$	-55 ~ 150	°C
Storage Temperature Range	$T_{stg}$	-55 ~ 150	°C
High Temperature(tin solder)	$T_L$	300	°C

### 4.2 Thermal Characteristics

PARAMETER	SYMBOL	VALUE	UNIT
Thermal Resistance, Junction to Case-sink	$R_{thJC}$	1.67	°C/W
Thermal Resistance, Junction to Ambient	$R_{thJA}$	100	°C/W

**4.3 Electrical Characteristics** (Tc=25°C, unless otherwise noted)

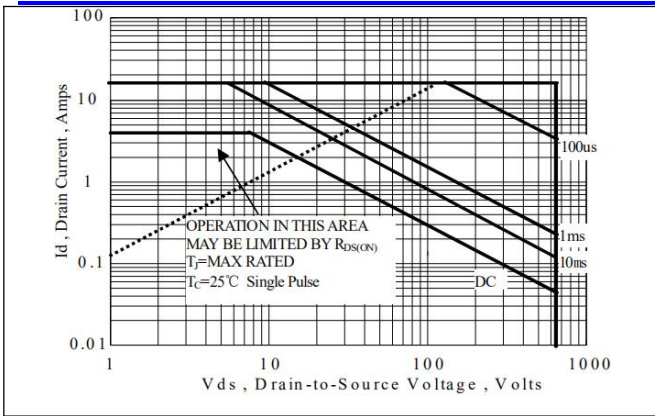
PARAMETER	SYMBOL	Test Condition	VALUE			UNIT
			MIN	TYP	MAX	
<b>Off Characteristics</b>						
Drain-source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	650	--	--	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =650V, V <sub>GS</sub> =0V, T <sub>C</sub> =25°C	--	--	1.0	μA
		V <sub>DS</sub> =520V, V <sub>GS</sub> =0V, T <sub>C</sub> =125°C	--	--	100	μA
Gate-to-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±30V, V <sub>DS</sub> =0V	--	--	±100	nA
<b>On Characteristics</b> (Note 3)						
Gate threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2.0	--	4.0	V
Drain-source on Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =2.5A	--	1.9	2.4	Ω
<b>Dynamic Characteristics</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1.0MHz	--	615	--	pF
Output Capacitance	C <sub>oss</sub>		--	55	--	
Reverse Transfer Capacitance	C <sub>rss</sub>		--	6.88	--	
Turn-on Delay Time	T <sub>d(on)</sub>	I <sub>D</sub> =5A, V <sub>DD</sub> =325V, V <sub>GS</sub> =10V, R <sub>G</sub> =10Ω	--	13	--	ns
Turn-on Rise Time	t <sub>r</sub>		--	8.8	--	
Turn-off Delay Time	T <sub>d(off)</sub>		--	25	--	
Turn-off Fall	t <sub>f</sub>		--	9.5	--	
Total Gate Charge	Q <sub>g</sub>	I <sub>D</sub> =5A, V <sub>DD</sub> =520V, V <sub>GS</sub> =10V	--	17.3	--	nC
Gate-to-Source Charge	Q <sub>gs</sub>		--	2.4	--	
Gate-to-Drain("Miller")C harge	Q <sub>gd</sub>		--	10.3	--	
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>FSD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =5A	--	--	1.5	V
Continuous Source Current (BodyDiode) (Note 3)	I <sub>S</sub>		--	--	5	A
Reverse Recovery Time	trr	T <sub>J</sub> =25°C, I <sub>F</sub> =5A,	--	390	--	ns
Reverse Recovery Charge	Q <sub>rr</sub>	dI <sub>F</sub> /dt=100A/μS, V <sub>GS</sub> =0V	--	1600	--	nC

Notes:

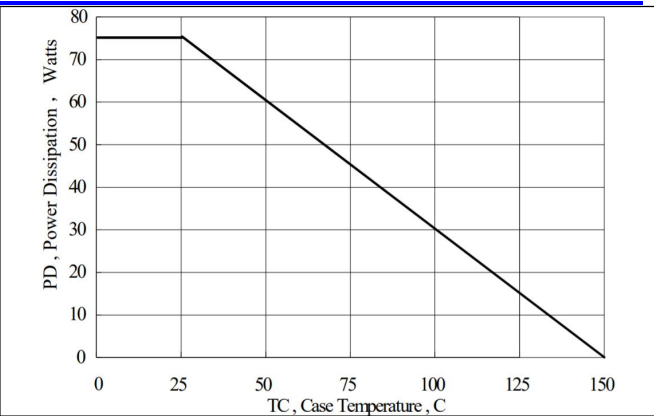
- 1: Repetitive rating, pulse width limited by maximum junction temperature.
- 2: Surface mounted on FR4 Board, t≤10sec.
- 3: Pulse width ≤ 300μs, duty cycle ≤ 2%.
- 4: L=10 mH, I<sub>D</sub>=6.8A, V<sub>DD</sub>=50V, Start T<sub>J</sub>=25°C.

**5 Typical Test Circuit and Waveform**

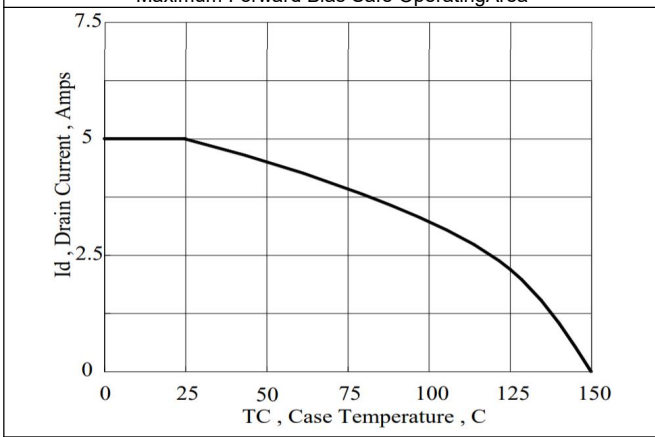
<p style="text-align: center;">Gate Charge Test Circuit</p>	<p style="text-align: center;">Gate Charge Waveforms</p>
<p style="text-align: center;">Resistive Switching Test Circuit</p>	<p style="text-align: center;">Resistive Switching Waveforms</p>
<p style="text-align: center;">Diode Reverse Recovery Test Circuit</p>	<p style="text-align: center;">Diode Reverse Recovery Waveform</p> $E_{AS} = \frac{I_{AS}^2 L}{2}$
<p style="text-align: center;">Unclamped Inductive Switching Test Circuit</p>	<p style="text-align: center;">Unclamped Inductive Switching Waveform</p>



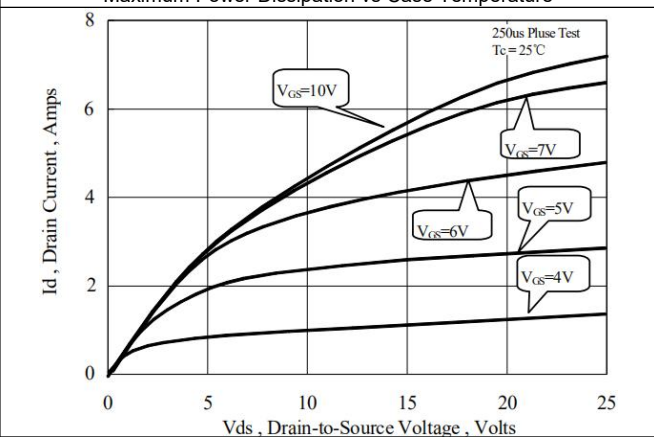
Maximum Forward Bias Safe Operating Area



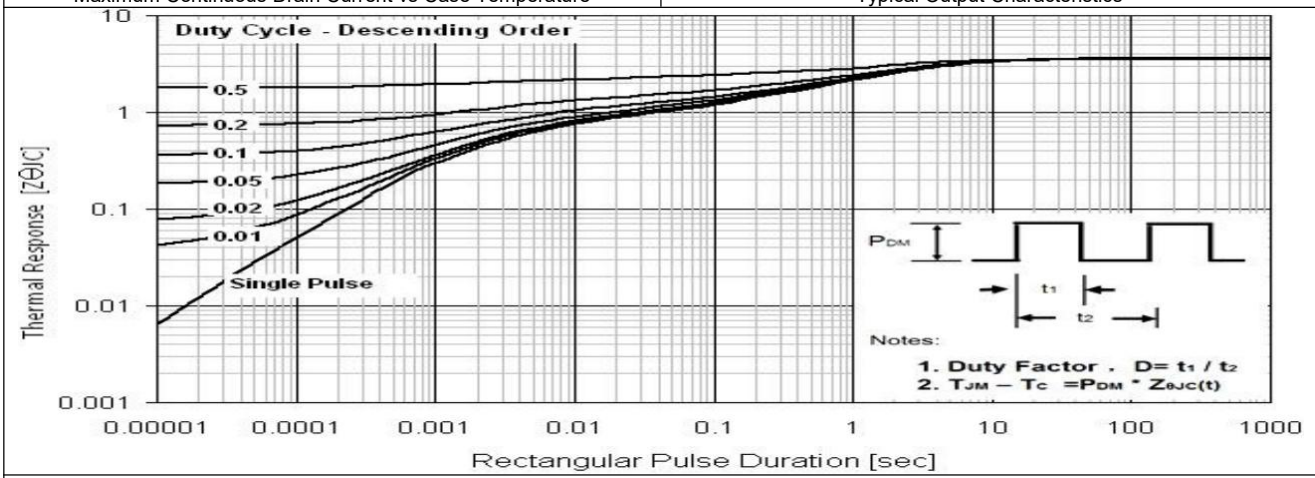
Maximum Power Dissipation vs Case Temperature



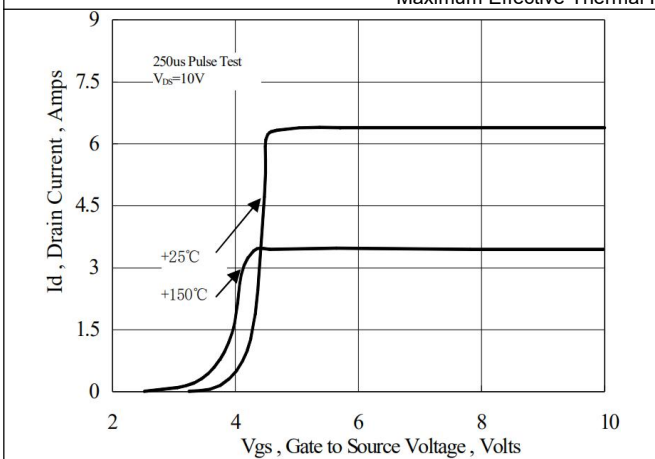
Maximum Continuous Drain Current vs Case Temperature



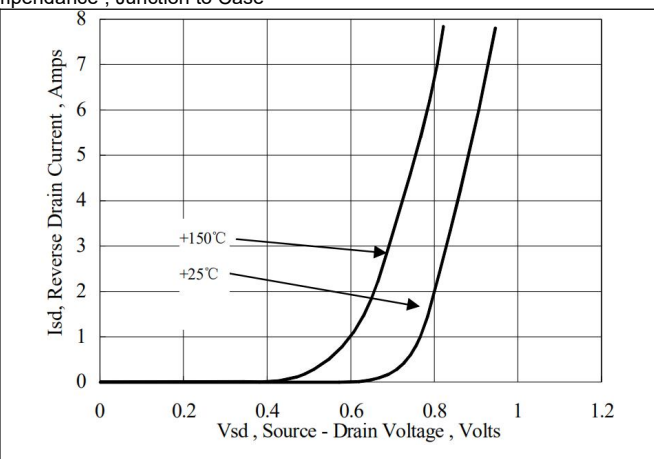
Typical Output Characteristics



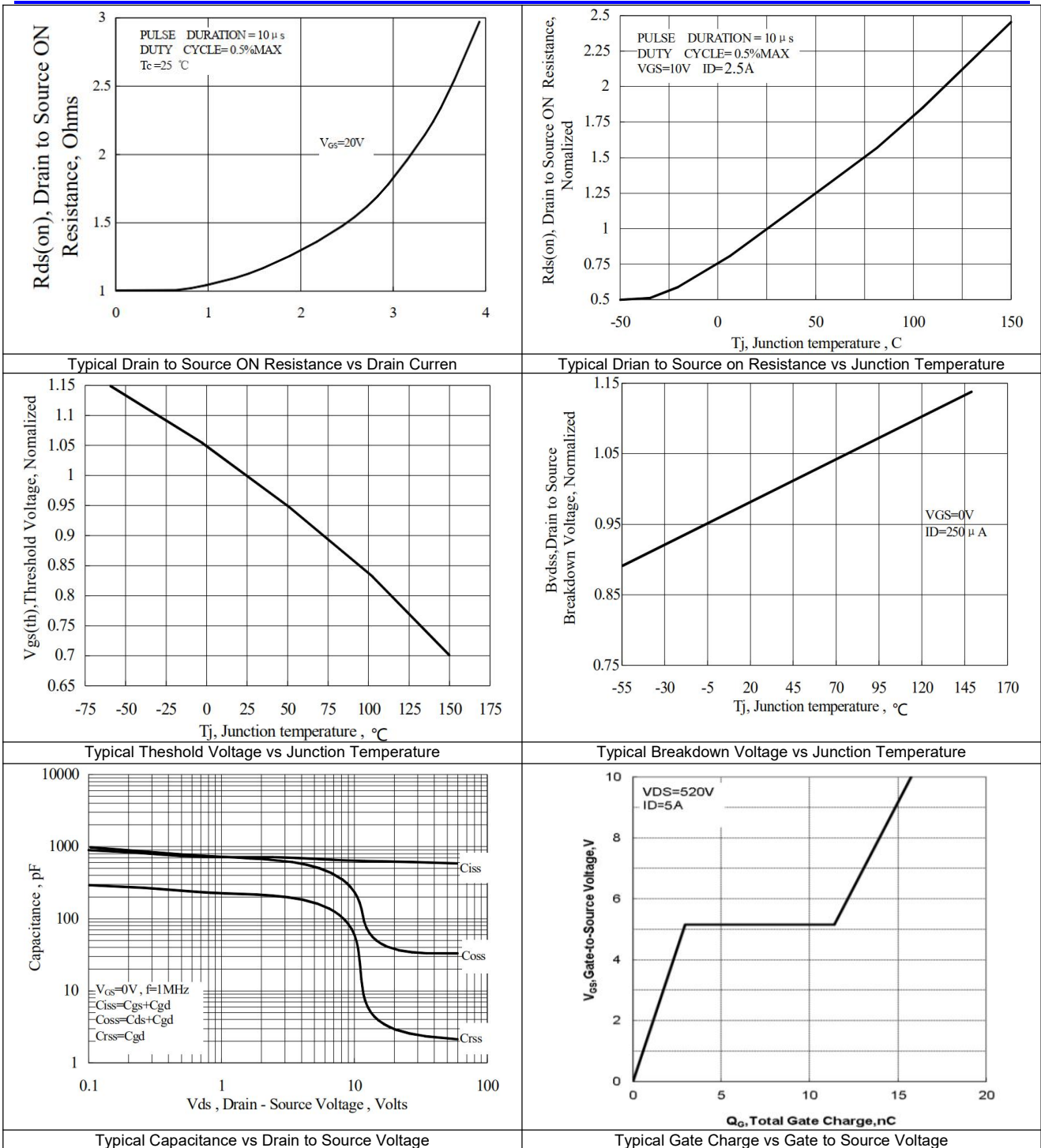
Maximum Effective Thermal Impedance , Junction to Case



Typical Transfer Characteristics



Typical Body Diode Transfer Characteristics

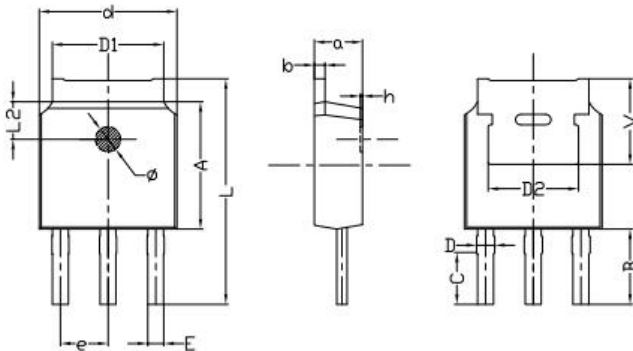


## 6 Product Specifications and Packaging Models

Product Model	Package Type	Mark Name	RoHS	Package	Quantity
B5N65	TO-251B	B5N65	Pb-free	Braid	3000/disc

## 7 Dimensions

### TO-251B PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	min.	max.	min.	max.
a	2.20	2.40	0.087	0.0946
b	0.46	0.58	0.018	0.023
C	2.45	2.65	0.097	0.104
D	0.80	0.90	0.032	0.035
d	6.50	6.70	0.2561	0.2640
D1	5.10	5.46	0.201	0.215
D2	4.73	4.93	0.1864	0.1942
A	6.00	6.20	0.2364	0.2443
e	2.186	2.386	0.0861	0.0940
L	10.40	11.00	0.4098	0.4334
B	3.50	3.70	0.1379	0.1458
L2	1.50	1.70	0.0591	0.0670
Φ	1.10	1.30	0.0433	0.0512
h	0.00	0.30	0.0000	0.0118
V	5.25	5.45	0.2069	0.2147
E	0.60	0.80	0.0236	0.0315

## 8 Attentions

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- Product promotion is endless, our company will be dedicated to provide customers with better products.

## 9 Appendix

Revision history:

Date	REV.	Description	Page
2021.05.09	1.0	Original	
2022.1.20	1.1	Modify company name	ALL